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Remarks

Applicant and his representatives wish to thank Examiner Pert for the examination of the present application and the explanations in the Office Action dated October 28, 2005. Claims 1-11 are active in the present application.

The present invention relates to a method for fabricating a semiconductor device. The method (as set forth in Claim 1) generally includes the steps of (a) forming a nitride layer on an interlayer insulating layer, (b) forming a photoresist layer on the nitride layer, (c) forming a photoresist pattern from the photoresist layer, the photoresist pattern having a thickness that depends on a thickness and an etch rate of the interlayer insulating layer and an etch rate of the photoresist pattern, (d) etching the nitride layer using the photoresist pattern as a mask, (e) etching the interlayer insulating layer together with the photoresist pattern, and (f) setting an etch stop point as a point at which the photoresist pattern is removed by etching. Alternatively, with respect to independent claim 10, the etch stop point is set at a point at which the nitride layer is exposed.

With respect to independent Claim 5, the method generally includes the steps of (a) forming a first mask layer on an etch target layer, (b) forming a second mask layer on the first mask layer, (c) forming a first mask pattern by selectively etching the second mask layer, the first mask pattern having a thickness that depends on a thickness and an etch rate of the etch target layer and an etch rate of first mask pattern, (d) forming a second mask pattern by etching the first mask layer using the first mask pattern as a mask, (e) etching the etch target layer together with the first mask pattern, wherein the first mask pattern is etched using the second mask pattern as a mask, and (f) setting an etch stop point as a point at which the first mask pattern is removed by etching. Alternatively, with respect to independent Claim 11, the etch stop point the etch stop point is set at a point at which the second mask pattern is exposed.

A person skilled in the art is capable of using the present invention based on the original specification without undue experimentation. Furthermore, the subject matter of the claims is described in the specification in such as way as to reasonably convey to one skilled in the art that

the inventors had possession of the claimed invention. Consequently, the present claims are enabled and patentable.

The Rejections of Claims 1-11 under the Enablement Requirement of 35 U.S.C. § 112, First Paragraph

The rejection of Claims 1-11 under 35 U.S.C. § 112, first paragraph is improper, and should be withdrawn. "The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation." *United States v. Telectronics, Inc.*, 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988) (see MPEP § 2164). The subject matter of the present claims 1, 5, 10 and 11 is described in the original specification in such a way as to reasonably convey to one skilled in the art that the inventor had possession of that subject matter at the time the application the was filed. In addition, a person skilled in the art is capable of using the present invention based on the original specification without undue experimentation. In particular, one skilled in the art of semiconductor manufacturing (and, in particular, etching material layers in semiconductor devices using masks) would readily understand from the application as originally filed how to make and use the invention, ***without reference to specific materials, etchants or etch processes*** (see, e.g., paragraphs 7 and 9, pages 3-4 of the accompanying Declaration of Jong-chul Lim; emphasis added). Accordingly, the subject matter of the present claims 1, 5, 10 and 11 are fully enabled by the application as filed (see paragraph 19, page 6 of the accompanying Declaration of Lim).

The Examiner appears to understand at least part of the inventive concept as recited in claims 1, 5, 10 and 11 (see, e.g., the first full paragraph on page 5 of the Office Action dated May 12, 2006 and paragraph 8, page 3 of the Declaration of Lim). At least part of the inventive concept involves recognizing that a second mask pattern (e.g., a nitride layer as recited in claims 1 and 10, or a "hard mask" as identified by the Examiner on page 5 of the Office Action) can be used to set an etch stop point for (simultaneously) etching a first mask pattern (e.g., a photoresist pattern as recited in claims 1 and 10, or a "photoresist" as identified by the Examiner on page 5

of the Office Action) on the second mask pattern and an etch target layer (e.g., an interlayer insulating layer as recited in claims 1 and 10, or "an insulating layer" as identified by the Examiner on page 5 of the Office Action), by use of a point at which either the first mask pattern is removed by etching (e.g., claims 1 and 5) or the second mask pattern is exposed (e.g., claims 10 and 11; see also paragraph 8, page 3 of the Declaration of Lim).

One skilled in the art of semiconductor manufacturing (and, in particular, etching material layers in semiconductor devices using masks) would readily understand from the application as originally filed how to make and use the invention, without reference to specific materials, etchants or etch processes, which generally depend on the recipe for a particular fabrication process (see paragraph 9, page 4 of the Declaration of Lim).

The application as originally filed discloses that the photoresist pattern is etched together with the interlayer insulating layer during an interlayer insulating layer etching process (see, e.g., paragraph [0013], page 3; and paragraph [0015], page 4). This disclosure is reflected in the language of the claims (e.g., ""etching the interlayer insulating layer together with the photoresist pattern..."; "etching the etch target layer together with the first mask pattern...," as recited in claims 1, 5, 10 and 11; see also paragraph 10, page 4 of the Declaration of Lim).

As is further disclosed in paragraph [0015] of the application as originally filed, the etching process is terminated by setting the time point when the photoresist pattern is entirely removed such that the nitride layer is exposed by the etching process. Also, as is further disclosed in paragraph [0013] of the application as originally filed (pages 3-4), the thickness of the photoresist pattern is determined by considering the thickness and etch rate of the interlayer insulating layer and the etch rate of the photoresist pattern (see paragraph 11, page 4 of the Declaration of Lim). ***One skilled in the art thus understands from paragraphs [0013] and [0015] of the application as originally filed that, from just the thicknesses and the etch rates of the interlayer insulating layer and the photoresist pattern, one can set an etch stop point for etching the photoresist pattern*** (the first mask pattern) ***and the interlayer insulating layer*** (the etch target layer) ***as the point at which*** (i) ***the photoresist pattern is removed by etching*** or (ii)

the nitride layer is exposed (see paragraph 12, page 4 of the Declaration of Lim; emphasis added).

It is within the abilities of those skilled in the art to determine a desired thickness for nearly any material used conventionally in semiconductor manufacturing from a deposition rate or growth rate and a length of the deposition (or growth) time. To obtain a sufficiently accurate rate, one skilled in the art generally determines a deposition rate or growth rate for a given material empirically, on a given apparatus (or equipment) and under a given set of operational conditions (usually starting with a default set of conditions for the given material and the given apparatus or equipment). Thus, ***it does not require undue experimentation to determine a thickness for nearly any given material used conventionally in semiconductor manufacturing*** (see paragraph 13, pages 4-5 of the Declaration of Lim; emphasis added).

Similarly, it is within the abilities of those skilled in the art to determine an etch rate for nearly any material used conventionally in semiconductor manufacturing using a particular apparatus (or equipment), a known etchant chemistry for a particular material, and a given set of operational conditions. To obtain a sufficiently accurate etch rate, one skilled in the art generally determines the etch rate for a particular material empirically, on a given apparatus (or equipment), using a given etchant chemistry (usually a default or recommended etchant chemistry for the particular material), under a given set of operational conditions (usually starting with a default set of conditions for the given apparatus or equipment, the given etchant chemistry, and the particular material). Thus, ***it does not require undue experimentation to determine an etch rate for nearly any material used conventionally in semiconductor manufacturing*** (see paragraph 14, page 5 of the Declaration of Lim; emphasis added).

It is known in the art that an end point of a process for etching a transparent or non-transparent material can be monitored using laser interferometry or laser reflectance, respectively (see, e.g., Wolf, S., Silicon Processing for the VLSI Era, vol. 1 (2000), Lattice Press, Sunset Beach, California; particularly the first paragraph of § 14.7.1, pp. 695-696, attached to the Declaration of Lim ["Wolf"]). It is further known in the art that both photoresists and a nitride layer (e.g., silicon nitride) can be used to monitor an end point of an etching process using

optical emission spectroscopy (Wolf, p. 697, attached hereto). Although these end point monitoring techniques may have limitations or other drawbacks, the limitations and/or drawbacks are known, and do not render the present invention inoperable (see paragraph 15, page 5 of the Declaration of Lim).

The application as originally filed includes a number of examples of how to make and use the invention. For example, paragraph [0016] on page 4 of the application as originally filed states that when the respective etch rates of the interlayer insulating layer and the photoresist pattern are about 5000 Å/min and about 1800 Å/min, the interlayer insulating layer is formed to have a thickness of about 7500 Å, and the photoresist pattern (after etching the nitride layer) has a thickness of about 2500 Å. As a result, the photoresist pattern is entirely removed when about 7000 Å of the interlayer insulating layer is etched, thereby exposing the nitride layer (see paragraph 16, pages 5-6 of the Declaration of Lim; emphasis added). Therefore, ***as described in the present application***, when the second (photoresist) mask layer is thick enough, it can be used as an etching mask (e.g., to etch the first mask [nitride] layer, see paragraph [0014] of the original description), and when etching time is long enough, the photoresist layer can be completely etched along with the target (insulating) layer (e.g., by exposing the first mask [nitride] layer to determine the etch end point; see, e.g., paragraph [0015] of the original description, and paragraph 17, page 6 of the Declaration of Lim; emphasis added).

Therefore, it is well within the abilities of a person skilled in the art to select specific mask materials (e.g., photoresists and nitrides), specific etch target (e.g., interlayer insulator) materials, and specific etchant(s) and/or etch processes (as well as to select specific thicknesses of each of the materials consistent with the easily determined deposition/growth rates thereof) in order to carry out the steps -- and obtain the results -- of the present invention (see paragraph 18, page 6 of the Declaration of Lim). Accordingly, the subject matter of claims 1, 5, 10 and 11 are fully enabled by the application as filed (see paragraph 19, page 6 of the accompanying Declaration of Lim).

Accordingly, Claims 1-11 are fully enabled, and the rejection of Claims 1-11 under 35 U.S.C. § 112, first paragraph should be withdrawn.

Atty. Docket No. OPP031054US
Serial No: 10/734,818

A number of points in the Office Action of May 12, 2006 should be addressed to ensure a complete and adequate record.

First, the assertion that the thicknesses recited in claims 2-3 would not work with the photoresist and insulating layer in U.S. Patent No. 4,376,672 to Wang et al. (hereinafter, "Wang") is incorrect. With regard to the photoresist thicknesses of claim 3, the accompanying Declaration of Lim explains that one skilled in the art understands that an etch stop point for etching the photoresist pattern (the first mask pattern) and the interlayer insulating layer (the etch target layer) can be set from just the thicknesses and the etch rates of the interlayer insulating layer and the photoresist pattern (see paragraph 12 of the Declaration of Lim and paragraphs [0013] and [0015] of the application as originally filed). As a result, if one is given a thickness for the photoresist pattern (claim 3), one skilled in the art can, ***without undue experimentation***, determine etch rates for the photoresist pattern and the interlayer insulating layer (see paragraph 14, page 5 of the Declaration of Lim; emphasis added), then determine, again ***without undue experimentation***, an appropriate thickness of the interlayer insulating layer (see paragraph 13, pages 4-5 of the Declaration of Lim; emphasis added). Thus, one skilled in the art can readily find working combinations of materials using available resources using the photoresist thicknesses recited in claim 3, including those disclosed by Wang, based on knowledge of the relative etch rates of the photoresist and insulator materials.

In addition, with regard to the nitride layer thicknesses recited in claim 2, the specification teaches that the nitride layer may be used as a mask when over-etching the interlayer insulating layer (see, e.g., paragraphs [0019] and [0024] of the specification as originally filed). The nitride layer thicknesses recited in claim 2 (see also paragraph [0025] of the specification as originally filed) are presumably useful and enabled for this purpose. Thus, one skilled in the art can readily find working combinations of materials using available resources using the thicknesses recited in claims 2-3.

M.P.E.P. § 2164.02 does, in fact, state that working examples are not required for enablement:

> "The specification need not contain an example if the invention is otherwise disclosed in such manner that one skilled in the art will be able to practice it without an undue amount of experimentation. In re Borkowski, 422 F.2d 904, 908, 164 USPQ 642, 645 (CCPA 1970)."
>
> "When considering the factors relating to a determination of non-enablement, if all the other factors point toward enablement, then the absence of working examples will not by itself render the invention non-enabled. In other words, lack of working examples or lack of evidence that the claimed invention works as described should never be the sole reason for rejecting the claimed invention on the grounds of lack of enablement."

Thus, the inference at page 4, second paragraph, that M.P.E.P. § 2164.02 sets forth "facts" requiring one or more working examples for enablement is simply wrong.

Finally, the eight factors to be considered when determining whether there is sufficient evidence to support a determination that a disclosure does not satisfy the enablement requirement and whether any necessary experimentation is "undue" include, but are not limited to:

(A) The breadth of the claims;

(B) The nature of the invention;

(C) The state of the prior art;

(D) The level of one of ordinary skill;

(E) The level of predictability in the art;

(F) The amount of direction provided by the inventor;

(G) The existence of working examples; and

(H) The quantity of experimentation needed to make or use the invention based on the content of the disclosure.

The Office Action of May 12, 2006, appears to focus on one of these factors, the existence of working examples (and more specifically, a lack of specific materials and etch processes). However, the specification does, in fact, include working examples (see paragraph [0016], page 4 of the application as originally filed, and paragraph 16 of the Declaration of Lim).

"*A single working example* in the specification for a claimed invention ***is enough to preclude a rejection which states that nothing is enabled*** since at least that embodiment would be enabled." M.P.E.P. § 2164.02; emphasis added. Thus, the one "undue experimentation" factor on which the Office Action focuses actually supports a finding of enablement.

Furthermore, the accompanying Declaration of Lim includes evidence establishing that specific materials and etch processes are not relevant to a determination of whether the present disclosure satisfies the enablement requirement. One skilled in the art understands from paragraphs [0013] and [0015] of the application as originally filed that, ***from just the thicknesses and the etch rates of the interlayer insulating layer and the photoresist pattern***, one can set an etch stop point for etching the photoresist pattern (the first mask pattern) and the interlayer insulating layer (the etch target layer) as the point at which (i) the photoresist pattern is removed by etching or (ii) the nitride layer is exposed (paragraph 12 of the Declaration of Lim; emphasis added), and that it is within the abilities of those skilled in the art to determine a desired thickness and an etch rate for nearly any material used conventionally in semiconductor manufacturing (paragraphs 13-14 of the Declaration of Lim). This disclosure from paragraphs [0013] and [0015] of the specification is reflected in the language of the claims (e.g., "etching the interlayer insulating layer together with the photoresist pattern..."; "etching the etch target layer together with the first mask pattern..."). ***"As long as the specification discloses at least one method for making and using the claimed invention that bears a reasonable correlation to the entire scope of the claim, then the enablement requirement of 35 U.S.C. 112 is satisfied.*** In re Fisher, 427 F.2d 833, 839, 166 USPQ 18, 24 (CCPA 1970)." M.P.E.P. § 2164.01(b); emphasis added. "If a statement of utility in the specification contains within it a connotation of how to use, and/or the art recognizes that standard modes of administration are known and contemplated, 35 U.S.C. 112 is satisfied. In re Johnson, 282 F.2d 370, 373, 127 USPQ 216, 219 (CCPA 1960); In re Hitchings, 342 F.2d 80, 87, 144 USPQ 637, 643 (CCPA 1965). See also In re Brana, 51 F.2d 1560, 1566, 34 USPQ2d 1437, 1441 (Fed. Cir. 1993)." M.P.E.P. § 2164.01(c). The specification discloses how to make and use the invention, and that disclosure is reflected in the language of the claims. Therefore, the application complies with the enablement requirement of 35 U.S.C. § 112, first paragraph, and whether the present disclosure identifies specific

materials and etch processes is simply not relevant to a determination of compliance with or satisfaction of the enablement requirement.

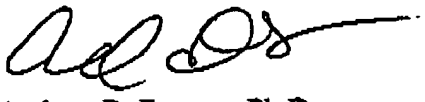
In view of the application's clear compliance with the enablement requirement of 35 U.S.C. § 112, first paragraph, a discussion of the remaining "undue experimentation" factors (and/or the remaining inaccuracies in the Office Action dated May 12, 2006) is moot.

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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